Hanover, October 6, 2004

X4

Statement in accordance with Article 19(1) PCT

The new claim 1 has been reworded such that it comprises technical features, and does not represent a purely mathematical method.

Claims 2 and 3 correspond to the renumbered claims 3 and 4.

The new claim 4 relates to an exemplary embodiment of the invention, which contains a look-up-table.

The new claim 5 relates to a circuit which carries out the method as claimed in claims 1 to 4.

Article 19

Translation of Article 19 claims

New Patent Claims

1. A method for formation of a histogram using accumulators which are associated with respective support points, wherein the range of the possible input values is subdivided into sub-ranges, which are bounded by two support values, wherein each support value has an associated accumulator, **characterized in that** a subtractor calculates the difference between the input value and a support value of the sub-range in which the input value is located, in that a first sharing factor is calculated from the difference, in that the complement value of the first sharing factor forms a second sharing factor, in that a multiplier multiplies the input value by the first and the second sharing factors, in that the products of the input values and of the sharing factors are accumulated by the accumulators which are associated with the support values, and in that a divider divides the accumulated values by the total number of sharing factors which have in each case been accumulated separately on the basis of the support values.

2. The method as claimed in claim 1, **characterized in that** the sharing factors are derived linearly from the differences.

3. The method as claimed in one of claims 1 or 2, **characterized in that** the sharing factors are derived from the differences by means of a non-linear function.

4. The method as claimed in claim 3, **characterized in that** the non-linear function is stored in a look-up-table.

5. A circuit for formation of a histogram with accumulators, which are associated with respective support points, wherein the range of the possible input values is subdivided into sub-ranges, which are bounded

by two support values, wherein each support value has an associated accumulator, **characterized in that** an input value is supplied via an input (VA) to a selector (3) by means of which a sub-range can be selected, which matches the input value, wherein an address signal (As) is applied to selection switches for selection of the associated accumulator, in that a subtractor (7) is provided by means of which the value of the lower support value in the sub-range can be subtracted from the input value, in that the difference (D) is supplied as an input signal to a look-up-table (8), whose output signal (D') is a first sharing factor, in that the first sharing factor is supplied to a first multiplier (10), to which a discrepancy value (DA) is supplied as a further factor, and whose output signal (Io) is supplied to a first accumulator (12), which is selected by the address signal (As), in that the output value (D') from the look-up-table (8) is supplied as a first counting variable (Co) to a first counting accumulator (13) which is selected by means of the address signal (As), in that a complement circuit (9) forms the complement of the output signal (D') from the look-up-table (8), wherein the complement is supplied as a second counting variable (Cu) to a second counting accumulator (13) which is selected by means of the address signal, in that the complement is supplied to a second multiplier (11), to which the discrepancy value (DE) is supplied as a further factor, and whose output signal (Iu) is supplied to a second accumulator (12), which is selected by the address signal (As), and in that a divider circuit (14) divides the contents of the first and second accumulators (12) by the contents of the respectively associated counting accumulators (13).